IN THE SPECIFICATION

Please amend the specification as follows:

Paragraph [0001] is amended as follows:

The invention relates to an apparatus and method for analysis and troubleshooting of electronic devices. More particularly, the present invention is an apparatus and method for [[the]] retrieving the contents of flip-flops within a chip at any given clock cycle through an external interface.

Paragraph [0003] is amended as follows:

Throughout the design and production of a device such as, but not limited to, a microprocessor, memory controller, peripheral interface, and communications interface, extensive testing occurs of the logic, design, prototype, and throughout the manufacturing process of the final product. For example, during the design phase of a microprocessor the circuitry and logic of the microprocessor are simulated and thoroughly tested. Further, once a prototype is built, diagnostics are run on the prototype that attempt to simulate the real world operations of the prototype and identify any possible problems in logic or manufacture that may exist. Once a device goes into manufacture, extensive testing is performed throughout the entire manufacturing process to ensure ~~assure~~ each component operates ~~components operating~~ properly. However, once a device, such as a chip, is assembled there is no method for analyzing the state of the chip at any given clock cycle. More specifically, no method or device exists for determining the values contained in flip-flops and registers for any given clock cycle once the chip is manufactured and fully assembled.

Paragraph [0016] is amended as follows:

Still referring to FIG. 1, a total of six devices are shown interfacing to a front-end bus 50. These devices include two processors 10, a memory controller 60 interfacing to memory 70, a universal serial bus (USB) interface 80, a small computer system interface (SCSI) 90, and a

communications interface 100. Each component illustrated in FIG. 1 is collectively referred to as device(s). Each device has a scan module 20 contained therein. The scan modules 20 are incorporated in each device during manufacturing in order to test the respective device during the manufacturing process. Until the example embodiments of the present invention, the scan module 20 was not used after the device had [[has]] been manufactured. In normal operation of the digital electronic system, the scan module 20 would not be active and would not influence the operation of the digital electronic system. Communications with the scan module 20 may utilize an external event trigger signal 30 and scan chain signal 40. Both the external event trigger signal 30 and scan chain signal 40 may be incorporated in the baseboard (motherboard) in which the front end [[and]] bus 50 would be embedded and the devices shown in FIG. 1 attached thereto. As will be discussed in further detail ahead, upon receipt of an external event trigger signal 30 the scan module 20 would freeze the operation of the device and begin serial transmission of the contents of the device over scan chain signal 40.

Paragraph [0018] is amended as follows:

FIG. 3 is a block diagram illustrating the connections between the scan module 20 and device core 300 in an example embodiment of the present invention. As previously discussed, scan module 20 would be contained within device ~~devices~~ 310 illustrated in, but not limited to, FIG. 1. In the case where device 310 is a processor 10, as illustrated in FIG. 1, device core 300 may contain all the elements required by a processor 10 to perform its functions. Contained within scan module 20 would be a synchronous scan control module 340 which would receive the external event trigger signal 30 from the external test equipment 200, previously discussed in reference to FIG. 2. Upon receipt of the external event trigger signal 30 the synchronous scan control module 340 would generate a synchronous scan command 350 to the device core 300 that would cause the device core to cease operations and freeze the contents of any flip-flops or registers contained therein. The synchronous scan control module 340 would receive the same operational clock signal 320 used to synchronize all devices 310 in the digital electronic system illustrated in FIG. 1. This operational clock signal 320 would also be input to device core 300 so that the device core 300 of devices 310 would be synchronized with the other devices 310 in the computer system shown in FIG. 1. In addition, the scan clock signal 330 would be input to the

device core and scan module 20 from the external test equipment 330 in order to synchronize the transmission of data from the device core to the external test equipment 200 via the scan chain signal 40.

Paragraph [0019] is amended as follows:

FIG. 4 is a block diagram illustrating the operation of the device core 300 connected to a synchronous scan control module 340 via synchronous scan command signal 350 in an example embodiment of the present invention. In the example embodiment provided in FIG. 4, the synchronous scan control module 340 has not received an [[in]] external event trigger 30 from the external test equipment 200. Therefore, the synchronous scan command signal 350 has not been activated and serial output from the scan chain signal 40 is not being transmitted to the external test equipment 200. It should be noted that the device core 300 could be operating as required by the nature of device 310. Flip-flops 400, 410, 430, 440 may be interconnected as illustrated in FIG. 4 utilizing combinational logic units 480 and 490. Combinational logic units 480 and 490 would receive data from flip-flops 400 and/or 410 and transmit the data to flip-flops 410 and 440. As would be appreciated by one of ordinary skill in the art, the precise interconnection of flip-flops 400 through 440 would depend upon the specific design of device core 300 and device 310. Therefore, FIG. 4 is provided merely as an example of how a device core 300 may be designed. Further, output from flip-flop 410 ~~maybe~~ may be redirected ~~with in~~ within device core 300 via signal 450 and output from flip-flop 440 ~~maybe~~ may be redirected within device core 300 via signal 460.

Paragraph [0021] is amended as follows:

Still referring to FIG. 5, upon receipt of external event trigger signal 30 the synchronous scan control module 340 would generate a synchronous scan command signal 350 that would cause all flip-flops within device core 300 to hold operations, retain contents, and serially transmit ~~transmits~~ the contents of each flip-flop to external test equipment 200 via scan chain signal 40. As previously discussed the mechanism of operation of the synchronous scan control module 340 remains unchanged from that used in the manufacturing process. However, using the external event trigger signal 30 and receiving data for the scan chain signal 40, it is possible

for external test equipment 200 to be utilized in a non-manufacturing environment and after the device 310 has been completed and possibly installed in a digital electronic system. Once scan mode operations have commenced, signals 450 and 460 would not be utilized even though the physical connections remain.

Paragraph [0023] is amended as follows:

FIG. 6 is a flowchart of the process utilized to initiate a scanning of all flip-flops in a device 310 and the storing and reporting of the contents of the flip-flops in an example embodiment of the present invention. Processing begins execution in operation 600 and immediately proceeds to operation 610. In operation 610 device 310 would be embedded in a digital electronic system, as illustrated in FIG. 1, and maybe executing some function. In operation [[320]] 620 it is determined if an external event trigger signal 30 has occurred. If an external event trigger signal 30 has not occurred then processing loops back to operation 610. However, if an external event trigger signal 30 has occurred then processing proceeds to operation 630. The external event trigger signal 30 may be generated by external test equipment 200 and received by the synchronous scan control module 340. In operation 630, the synchronous scan control module 340 would set the synchronous scan command signal 350 to an on state. Processing then proceeds to operation 640 [[were]] where the scan mode is set on and the flip-flops in the device core 300 are held at a pre-scan state. The scan clock signal 330 is utilized to control the flip-flops from this point forward so that the device 310 is now synchronized with the external test equipment 200. In operation 650, the flip-flops ~~transmits~~ transmit serially their contents to the external test equipment 200. Thereafter, in operation 660 the external test equipment 200 receives, stores, and reports the contents of the flip-flops received to the user. Processing then proceeds to operation 670 where processing terminates.